CLAIMS

1. A method for forming in monolithic form a DRAM-type memory, including the steps of:

forming, on a single-crystal semiconductor substrate, parallel strips including a lower insulating layer, a strongly-conductive layer, a single-crystal semiconductor layer, and an upper insulating layer;

digging, perpendicularly to the strips, into the upper insulating layer and into at least a portion of the semiconductor layer, first and second parallel trenches, each of the first and second trenches being shared by neighboring cells;

forming, in each of the first trenches, a first conductive line according to the strip width;

forming, in each of the second trenches, a pair of second distinct parallel conductive lines, insulated from the layers peripheral to the second trench;

filling the first and second trenches with an insulating material;

removing the remaining portions of the upper insulating layer; and

depositing a conductive layer,

wherein the first and second trenches are dug into the upper insulating layer and at least a portion of the semiconductor layer so that the first trenches have a minimum width, and the second trenches have a width which is twice that of the first trenches, two neighboring trenches being separated by a minimum interval, each first trench being surrounded with two second trenches and each second trench being surrounded with two first trenches.

2. The method of claim 1, wherein the forming of the parallel strips includes the steps of:

forming on a first single-crystal semiconductor substrate a single-crystal semiconductor layer resting on a first insulating layer;

forming, on the semiconductor layer, a strongly-conductive layer, then a second insulating layer;

digging parallel trenches in the second insulating layer, the strongly-conductive layer, and the semiconductor layer, to partially expose the first insulating layer;

turning over and gluing the structure thus obtained on a second substrate; and

removing the first substrate, whereby the first insulating layer becomes the upper layer of the structure thus formed and the second insulating layer becomes the lower layer underlying the semiconductor layer.

3. The method of claim 1, wherein the first and second trenches are dug into to maintain between the strongly-conductive layer and the bottom of each of the first and second trenches a given thickness of the semiconductor layer.

4. The method of claim 1, wherein the first and second trenches are dug into to partially expose the strongly-conductive layer.

5. The method of claim 1, including simultaneously forming the first conductive lines at the bottom of each first trench and the pairs of second insulated conductive lines at the bottom of the second trenches.

6. The method of claim 5, wherein the simultaneous forming of the first lines and of the pairs of second lines at the bottom of the first and second trenches includes the steps of:

depositing at the bottom and on the walls of the first and second trenches an insulating layer;

conformally depositing a conductive material to at least fill the first trench; and

removing the conductive material from the surface of the first insulating layer.

7. The method of claim 5, wherein the lines formed at the bottom of the first trenches are not insulated from the peripheral semiconductor and/or conductor layers.

8. The method of claim 7, including the steps of:

conformally depositing an insulating material at the bottom and on the walls of the first and second trenches;

conformally depositing a first sub-layer of a conductive material;

performing a directional bombarding so that the conductive material is only bombarded on its sides in the second trenches;

removing by selective etching the sole non-bombarded portions of the conductive material in the first trenches;

removing the portions thus exposed of the insulating material previously deposited at the bottom of the first and second trenches;

depositing a second sub-layer of the conductive material to at least fill the first trenches; and

removing the conductive material from the surface of the first insulating layer.

9. The method of claim 1, including, after the step of deposition of a conductive layer, the steps of:

level trimming, which results in the forming, between a first and a second neighboring trenches, of independent conductive surfaces in contact with the surface of the semiconductor layer;

depositing over the entire structure a thin dielectric with a high permittivity; and

depositing over the entire structure a conductive layer.

10. A DRAM, including:

parallel strips formed of the stacking, on a single-crystal semiconductor substrate, of an insulating layer of a strongly-conductive line, and of a semiconductor layer;

first conductive lines running perpendicularly to the strips, each in a first relatively thin trench dug into at least a portion of the semiconductor layer;

pairs of second conductive lines parallel to each other and to the first lines, each pair of second lines running in a second relatively wide trench dug into at least a portion of the semiconductor layer between two first trenches; and

conductive surfaces of unity area resting on the semiconductor layer, these surfaces being defined at the surface of the strips by the intervals separating a first and a second neighboring strips.

11. The DRAM of claim 10, wherein the first and second trenches do not reach the underlying strongly-conductive lines, the second lines being insulated with respect to the peripheral semiconductor layer and forming the word lines of the memory, the strongly-conductive lines forming the bit lines of the memory, and the surfaces of unity area forming first individual electrodes of the memory points of the memory.

12. The DRAM of claim 11, wherein the first lines are reference biasing lines of the semiconductor layer, independent from the line pairs running in the second trenches.

13. The DRAM of claim 11, wherein the first lines are insulated from at least the peripheral semiconductor layer.